WHAT IS CLAIMED IS:

1. A method for provisionally determining quantity and positions of a plurality of power supply pads when designing a semiconductor integrated circuit including a core section provided with a plurality of nodes and the plurality of power supply pads, with each power supply pad being connected to the core section via an IO buffer, wherein each IO buffer has a predetermined current capacity, the method comprising:

performing a power supply network analysis of the core section based on power consumption information of the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes;

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculating current values of the power supply pads from the current values between the nodes;

determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer; and

eliminating or adding at least one power supply pad in accordance with the result of the determination.

2. The method according to claim 1, wherein said calculating voltage values of the nodes includes calculating IR drop values between the nodes based on the voltage value of each node and suspending subsequent processing when any one of the calculated IR drop values exceeds a predetermined maximum IR drop value.

3. The method according to claim 1, wherein said

performing a power supply network analysis includes modeling the core section as a plurality of equivalent circuits electrically equivalent to one another, each equivalent circuit including a resistor and a current source, and performing the power supply network analysis on the modeled core section.

4. The method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power supply wire density in the core section.

5. The method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power consumption of the core section.

6. The method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of the current values of the power supply pads.

7. The method according to claim 1, wherein the designed semiconductor integrated circuit is provided with a plurality of pads including the power supply pads, the method further comprising:

initially defining all of the pads as power supply pads at which the potential is the same,

wherein said eliminating or adding at least one power supply pad includes eliminating a power supply pad of which current value is less than the current capacity.

8. The method according to claim 7, further comprising:

determining whether a completion condition is satisfied after deleting the at least one power supply pad, wherein subsequent processing is terminated when the completion condition is satisfied, and said performing a power supply network analysis is executed again when the completion condition is not satisfied.

9. The method according to claim 7, wherein said initially defining all of the pads includes selecting from all of the power supply pads a power supply pad that has a determined location to use the selected power supply pad as a reference pad, said eliminating or adding at least one power supply pad includes checking whether deletion of every one of the power supply pads excluding the reference pad is possible.

10. The method according to claim 9, wherein said eliminating or adding at least one power supply pad includes distributing the current value of one power supply node, excluding the reference pad, at a predetermined ratio to the reference pad, comparing the current value of the reference pad subsequent to the distribution with the current capacity, and determining whether deletion of the power supply is possible in accordance with the comparison result.

11. A method for provisionally determining quantity and positions of a plurality of power supply pads before detailed design of a semiconductor integrated circuit, wherein the semiconductor integrated circuit includes a core section provided with a plurality of nodes and a plurality of power supply pads, the method comprising:

initially defining all of the pads as power supply pads at which the potential is the same;

performing a power supply network analysis of the core

section based on power consumption information of the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes;

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculating current values of the power supply pads from the current values between the nodes;

determining whether there is a power supply pad for which current value is less than or equal to a predetermined current capacity; and

adding a new power supply pad near a power supply pad for which current value exceeds the predetermined current capacity, and assigning a power supply pad as another type of pad when the current value of that power supply pad is less than or equal to the predetermined current capacity.

12. A method for estimating the size of a core section of a semiconductor integrated circuit, wherein the core section includes a plurality of nets, each including a plurality of wires, the method comprising:

calculating the total net length of the wires of the nets and usable channel length of the core section by referring to circuit information and a layout parameter that are used to design the semiconductor integrated circuit, the total net length being the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires extending in a second direction perpendicular to the first direction, and the usable channel length being the sum of a channel length in the first direction and a channel length in the second direction;

calculating the total length of the first wires;

calculating the total length of the second wires; and

determining the size of the core section that satisfies conditions of the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction.

13. The method according to claim 12, further comprising:

determining whether the conditions are satisfied; and

changing the layout parameter and repeating said calculating the total net length of the wires of the nets and usable channel lengths, the total length of the first wires, and the total length of the second wires, and said determining the size of the core section until the conditions are satisfied.

14. The method according to claim 12, wherein the core section is provided with a plurality of wire layers, each wire layer including at least one circuit block, the nets are each arranged on one of the wire layers, each net having paths, the quantity of which is in accordance with the fan-out of the net, the layout parameter includes an aspect ratio of each circuit, and the circuit information includes the fan-out of each net, said calculating the total net length of the wires includes:

calculating an average path length of the wires in each net;

calculating the net length of each net based on the average path length and fan-out of each net to calculate the total net length of the nets; and

calculating the lengths of the first wires and the

lengths of the second wires based on the calculated total net length and the aspect ratio of each circuit block.

15. The method according to claim 12, wherein said calculating the usable channel length of the core section includes:

estimating the area of the core section;

calculating a routing prohibition channel length of each wire layer;

calculating the usable channel length of each wire layer from the routing prohibition channel length and a maximum channel usage rate, which is in accordance with the area of the estimated area, to calculate the total usable channel length of the wire layers;

calculating the usable channel length in the first direction by totaling the usable channel length of the first wire layers having wires arranged along the first direction; and

calculating the usable channel length in the second direction by totaling the usable channel length of the second wire layers having wires arranged along the second direction.

16. A method for estimating the size of a core section in a semiconductor integrated circuit provided with a plurality of circuit blocks and the core section, which includes a plurality of repeater cells arranged between the circuit blocks, the method comprising:

calculating the total area of the circuit blocks;

calculating the area of a wire region extending around each circuit block to receive wires in order to calculate the total area of the wire regions of the circuit blocks;

calculating the total area of the repeater cells; and

calculating the size of the core section by totaling the

total area of the circuit blocks, the total area of the wire regions, and the total area of the repeater cells.

17. The method according to claim 16, wherein the core section includes a plurality of wire layers, each wire layer including at least one circuit block, wherein said calculating the area of a wire region includes:

calculating a total quantity of routing channels in the circuit block of each wire layer;

calculating the quantity of usable routing channels in each wire layer; and

calculating the wire region area of each circuit block so that the total of the quantity of wires that is in accordance with the quantity of terminals in each block is equal to the quantity of usable routing channels in the wire layer of the circuit block.

18. The method according to claim 16, wherein said calculating the total area of the repeater cells includes multiplying the quantity of the repeater cells by the area of each repeater cell, the quantity of the repeater cells being calculated based on the average total area of each circuit block and the associated wire region, a repeater cell interval, the quantity of circuit blocks, the average-fan-out, and a Rent's exponent.

19. A method for estimating provisional wire capacitance in a semiconductor integrated circuit including a plurality of nets, each having a plurality of wires, the method comprising:

calculating an average path length for nets having the same fan-out by referring to circuit information and a layout parameter that are used to design the semiconductor integrated circuit;

calculating an average net length of the nets having the same fan-out based on the average path length calculated for nets having the same fan-out; and

estimating the provisional wire capacity for nets having the same fan-out based on the average net length and the capacity per unit length of the associated wires.

20. A method for estimating the size of a chip for a semiconductor integrated circuit provided with at least one core section and a plurality of power supply pads, the core section including a plurality of nets, each having a plurality of wires, and each of the power supply pads being connected to the core section via an IO buffer having a predetermined current capacity, the method comprising:

calculating the total net length of the wires of the nets and the usable channel length of the core section by referring to circuit information and a layout parameter that are used to design the semiconductor integrated circuit, the total net length being the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires extending in a second direction perpendicular to the first direction, and the usable channel length being the sum of a channel length in the first direction and a channel length in the second direction;

determining the size of the core section that satisfies conditions of the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction;

performing a power supply network analysis of the core section based on power consumption information of the core section and power supply wire resistance information, which

includes resistances between the nodes, to calculate voltage values of the nodes;

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculating current values of the power supply pads from the current values between the nodes;

determining whether there is a power supply pad for which current value exceeds the predetermined current capacity;

eliminating or adding a power supply pad in accordance with the determination result and determining the quantity and locations of the power supply pads to calculate the area of an IO region in accordance with the determined quantity; and

totaling the size of the core section and the area of the IO region.

21. An apparatus for designing a semiconductor integrated circuit including a core section provided with a plurality of nodes and a plurality of power supply pads, the core section having a plurality of nets, each including a plurality of wires, each power supply pad being connected to the core section via an IO buffer, wherein each IO buffer has a current capacity, the apparatus comprising:

a storage device which stores power consumption information of the core section and power supply wire resistance information, including resistances between the nodes; and

a data processor in communication with the storage device, in which the data processor:

performs a power supply network analysis of the core section by referring to the power consumption information and the power supply wire resistance information to calculate voltage values of the nodes;

calculates current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculates current values of the power supply pads from the current values between the nodes;

determines whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer; and

eliminates or adding a power supply pad in accordance with the result of the determination to determine the quantity and locations of the power supply pads.

22. An apparatus for designing a semiconductor integrated circuit having a core section provided with a plurality of nets, each including a plurality of wires, the apparatus comprising:

a storage device which stores circuit information and a layout parameter that are used to design the semiconductor integrated circuit; and

a data processor in communication with the storage device, in which the data processor:

calculates the total net length of the wires of the nets and the usable channel length of the core section by referring to the circuit information and the layout parameter, the total net length being the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires extending in a second direction perpendicular to the first direction, and the usable channel length being the sum of a channel length in the first direction and a channel length in the second direction; and

determines the size of the core section that satisfies conditions including the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction.

23. An apparatus for designing a semiconductor integrated circuit provided with a core section and a plurality of power supply pads, the core section including a plurality of nodes and a plurality of nets, each net having a plurality of wires, and each of the power supply pads being connected to the core section via an IO buffer having a predetermined current capacity, the apparatus comprising:

a storage device which stores power consumption information of the core section, power supply wire resistance information, which includes resistances between the nodes, and circuit information and a layout parameter that are used to design the semiconductor integrated circuit; and

a data processor in communication with the storage device, in which the data processor:

calculates the total net length of the wires of the nets and the usable channel length of the core section by referring to the circuit information and the layout parameter, the total net length being the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires extending in a second direction perpendicular to the first direction, and the usable channel length being the sum of a channel length in the first direction and a channel length in the second direction;

determines the size of the core section that satisfies conditions of the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction;

performs a power supply network analysis of the core section by referring to the determined size of the core section, the power consumption information, and the power supply wire resistance information to calculate voltage values of the nodes;

calculates current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculates current values of the power supply pads from the current values between the nodes;

determines whether there is a power supply pad for which current value exceeds the current capacity of the associated IO buffer; and

eliminates or adds a power supply pad in accordance with the result of the determination to determine the quantity and locations of the power supply pads.

24. A recording medium comprising computer instructions stored thereon for determining quantity and positions of a plurality of power supply pads in a semiconductor integrated circuit including a core section provided with a plurality of nodes, each power supply pad being connected to the core section via an IO buffer, wherein each IO buffer has a predetermined current capacity, the computer instructions when executed by a computer performing steps including:

carrying out a power supply network analysis of the core

section based on power consumption information of the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes;

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes;

calculating current values of the power supply pads from the current values between the nodes;

determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer; and

eliminating or adding at least one power supply pad in accordance with the result of the determination.

25. A recording medium comprising computer instructions stored thereon for estimating the size of a core section of a semiconductor integrated circuit, wherein the core section includes a plurality of nets, each including a plurality of wires, the computer instructions when executed by a computer performing steps including:

calculating the total net length of the wires of the nets and the usable channel length of the core section by referring to circuit information and a layout parameter that are used to design the semiconductor integrated circuit, the total net length being the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires extending in a second direction perpendicular to the first direction, and the usable channel length being the sum of a channel length in the first direction and a channel length in the second direction;

determining the size of the core section that satisfies conditions of the total net length being less than or equal to

the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction.